Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.   (currently amended) A data communication arrangement, comprising:

a transmit module adapted to convert parallel data words into a plurality of serial data streams, each of which is carried by a data-carrying line; and

a receive module comprising a plurality of first in first out buffers (FIFOs), each FIFO coupled to a data-carrying line and adapted to collect, for the data-carrying line, data carried from the transmit module by the data-carrying line, and adapted to detect therein a frequency compensation code and wherein each FIFO comprises a bit dedicated to a flag indicating an alignment status for the data collected in the FIFO, the flag ~~set~~ is set in response to the detected frequency compensation code, the receive module adapted to align the data carried from the transmit module in response to the flag.

2.   (original) The data communication arrangement according to claim 1, wherein the receive module continuously checks alignment between the serial data streams and autonomously corrects alignment between the serial data streams.

3.   (original) The data communication arrangement according to claim 1, wherein the receive module includes a retraining sequence delay circuit adapted to delay a retraining sequence request and provide a retry data transmit request in response to the frequency compensation codes to mitigate skew-caused re-training and configuration sequences.

4.   (original) The data communication arrangement according to claim 1, wherein the frequency compensation code is a Skip code.

5.   (original) The data communication arrangement according to claim 1, wherein the receive module includes at least one shift register adapted to shift the serial data stream by at least one bit in response to the frequency compensation code.

6.   (original) The data communication arrangement according to claim 1, wherein the receive module includes at least one bit-shift pointer adapted to shift the serial data by at least one bit in response to the frequency compensation code.

7.   (original) The data communication arrangement according to claim 6, wherein the receive module includes a direction indicator adapted to provide an indication of the shift direction for the bit-shift pointer.

8.   (currently amended) A data communication arrangement, comprising:
        a parallel word storage circuit having a plurality of parallel to serial conversion modules, each parallel to serial conversion module adapted to serially transmit a portion of the data from the parallel word storage circuit, each portion of data transmitted with an embedded frequency compensation code; and
        an alignment storage circuit having a plurality of serial to parallel conversion modules, each serial to parallel conversion module adapted to receive the portions of data from the parallel word storage circuit and each serial to parallel conversion module connected in parallel to a first in first out buffer (FIFO) comprising a bit dedicated to a flag indicating an alignment status for data collected in the FIFO, the flag ~~set~~ is set in response to detection of the frequency compensation code, the alignment storage circuit adapted to provide an alignment detection signal to a data shift circuit in response to the flag for each FIFO, and adaptively shift the parallel data output from the portions of data in response to the alignment detection signal.

9.   (original) The data communication arrangement according to claim 8, wherein the alignment storage circuit includes a retraining sequence delay module adapted to delay a retraining sequence request and provide a retry data transmit request in response to the frequency compensation code.

10. (original) The data communication arrangement according to claim 8, wherein the frequency compensation code is a Skip code.

11. (original) The data communication arrangement according to claim 10, wherein the SKIP codes are dropped and not placed into the FIFO.

12. (currently amended) A PCI Express bus receiver, comprising:

an alignment storage circuit having a plurality of serial to parallel conversion modules, each serial to parallel conversion module adapted to connect to a PCI Express bus line and convert a serial bit stream to parallel data words, and each serial to parallel conversion module connected in parallel to a first in first out buffer (FIFO) comprising a bit dedicated to a flag indicating an alignment status for data collected in the FIFO, the flag set is set in response to detection of the frequency compensation code, the alignment storage circuit adapted to provide an alignment detection signal to a data shift circuit in response to the flag for each FIFO, and adaptively shift the parallel data output from the serial bit stream in each serial to parallel conversion module in response to the alignment detection signal.

13. (original) The PCI Express bus receiver according to claim 12, wherein the alignment storage circuit continuously checks alignment between the plurality of serial to parallel conversion modules and autonomously corrects alignment between the plurality of serial to parallel conversion modules.

14. (original) The PCI Express bus receiver according to claim 12, wherein the alignment storage circuit includes a retraining sequence delay module adapted to delay a retraining sequence request and provide a retry data transmit request in response to the frequency compensation code.

15.   (original) The PCI Express bus receiver according to claim 12, wherein the alignment storage circuit uses the frequency compensation codes to automatically correct synchronization errors between the plurality of serial to parallel conversion modules.

16.   (original) The PCI Express bus receiver according to claim 12, wherein the alignment storage circuit includes at least one shift register adapted to shift the serial bit stream by at least one bit in response to the alignment detection signal.

17.   (original) The PCI Express bus receiver according to claim 12, wherein the alignment storage circuit includes at least one bit-shift pointer adapted to shift the serial data by at least one bit in response to the alignment detection signal.

18.   (original) The PCI Express bus receiver according to claim 17, wherein the alignment storage circuit includes a direction indicator adapted to provide an indication of the shift direction for the bit-shift pointer.

19.   (currently amended) A method for aligning multiple byte lanes, comprising:
        converting parallel data into a plurality of serial data streams, wherein the data streams are encoded with frequency compensation codes;
        transmitting serial data over a plurality of byte lanes;
        receiving serial data from a plurality of byte lanes, wherein each byte lane is coupled to a first in first out buffer (FIFO) adapted to receive the serial data, each FIFO comprising a bit dedicated to a flag indicating an alignment status for data collected in the FIFO, the flag set is set in response to detection of the frequency compensation code; and
        converting serial data streams from the plurality of byte lanes into parallel data, wherein the parallel data is aligned in response to the flag.

20.   (original) The method of claim 19, wherein the serial data is transmitted over a PCI Express bus.

21.   (original) The method of claim 19, wherein the serial data is transmitted over a fast Ethernet connection.

22.   (currently amended) A data communication arrangement, comprising:

a means for converting parallel data into a plurality of serial data streams, wherein the data streams are encoded with a frequency compensation code;

a means for transmitting serial data over a plurality of byte lanes;

a means for receiving serial data from a plurality of byte lanes, each byte lane connected to a first in first out buffer (FIFO) adapted to receive the serial data, each FIFO comprising a bit dedicated to a flag indicating an alignment status for data collected in the FIFO, the flag set is set in response to detection of the frequency compensation code; and

a means for converting serial data streams from a plurality of byte lanes into parallel data, wherein the parallel data is aligned in response to the flag.

23.   (original) The data communication arrangement of claim 22, wherein the frequency compensation code includes a comma code.

24.   (original) The data communication arrangement of claim 22, wherein the frequency compensation code includes a Skip code.

25.   (original) The data communication arrangement of claim 23, wherein the frequency compensation code includes a Skip code.

26.   (currently amended) A data communication arrangement, comprising:

a parallel circuit providing data symbols in serial form on a plurality of data lines, at least some of the data symbols including codes useful for frequency compensation; and

an alignment circuit comprising a plurality of first in first out buffers (FIFOs), each FIFO coupled to a data line and comprising a bit dedicated to a flag indicating an alignment status for data collected in the FIFO, the flag set is set in response to detection

of the frequency compensation code, the alignment circuit adapted to respond to the flag by aligning the data symbols and by removing the codes.

27. (original) The data communication arrangement according to claim 26, wherein the alignment circuit includes a retraining sequence delay module adapted to delay a retraining sequence request and provide a retry data transmit request in response to the codes.

28. (original) The data communication arrangement according to claim 26, wherein the alignment circuit includes a shift register adapted to reverse shift directions.

29. (original) The data communication arrangement according to claim 26, wherein the symbols include clock information.

30. (original) The data communication arrangement according to claim 26, wherein the codes are Skip codes.

31. (original) The data communication arrangement according to claim 26, wherein the alignment circuit adaptively shifts the serial data to detect the codes.

32. (currently amended) A method for de-skewing data, comprising:
    converting parallel data into a plurality of serial bit-streams;
    inserting frequency compensation codes into at least one of the bit-streams;
    transmitting the plurality of serial bit-streams over a plurality of parallel byte lanes, the parallel byte lanes susceptible to data skewing;
    receiving the plurality of serial bit-streams in a plurality of first in first out buffers (FIFOs), each FIFO receiving a serial bit-stream and comprising a bit dedicated to a flag indicating an alignment status for data collected in the FIFO, the flag set is set in response to detection of the frequency compensation code;
    performing a one-bit shift of the at least one of the bit-streams in response to the flag; and

dropping the frequency compensation codes from the at least one of the bit-streams before converting the plurality of serial bit-streams back into parallel data.

33. (original) The method of claim 32, further comprising determining a shift direction before performing the one-bit shift.

34. (original) The method of claim 32, further comprising determining a bit-count before performing a plurality of one-bit shifts, the number of shifts equal to the determined bit-count.

35. (original) The method of claim 32, wherein the frequency compensation codes are Skip codes.